Capacitive Wireless Power Transfer System with Double Matching Transformers for Reduced Stress and Extended ZVS Range

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***Abstract*—Capacitive power transfer uses an electric field to transmit power through physical isolation barrier utilizing capacitances formed by a couple of metal plates. Despite simplicity of the energy link structure, however, the physical dimension and low dielectric constant of the interface medium usually limits the effective link capacitance to be very small and nearly comparable to the main switch output capacitance in the transmitting circuit and thus narrows the soft-switching range. Unlike conventional approach which used very high operating frequency to handle these problems, this paper investigates a half-bridge inverter with double matching transformer networks to obtain required gain with decreased switching frequency and stable zero voltage switching operation for the load range. With mathematical analysis with fundamental harmonic approximation, design guideline is presented to provide a soft-switching scheme even in such a small link capacitances. Simulation and hardware implementation are performed to show that the proposed scheme ensures zero-voltage-switching up to 10% light load condition at switching frequencies that range from 244.5kHz to 345.6kHz for a 5W system equipped with a 256pF link capacitance and a 200pF switch output capacitance.**

Keywords—wireless power transfer; capacitive coupling; coupled electric field; zero voltage switching

I. INTRODUCTION

Capacitive power transfer (CPT) system uses an electric field instead of a magnetic field for an energy transmission through the isolation barrier [1]. It consists of a transmitting unit with a pair of transmitting conductors and a receiving unit with a pair of receiving conductors. The combination of conductors separated with a gap forms a link capacitor whose mechanical structure is simpler than the coil winding in conventional magnetic power transfer (MPT) system. Moreover, there is no magnetic flux unbounded nearby the interface medium and thus experience less EMI and metal obstacle problems.

However, despite these advantages, major limitations of CPT are usually caused by the link capacitance size. It is reported that ¼ mm air gap provides only 3.5pF/cm^2 [2]. Moreover, because there should be return path, the effective link capacitance is a series connection of the two individual link capacitors and thus becomes much smaller. Circuit designer should consider this small effective capacitance that makes the following challenges.

First, the small capacitance degrades the power factor. To tackle this problem, inductive components cancelling out the capacitance is needed. Secondly, low capacitance causes high voltage stress and increased switching frequency to process a given power. Such a high voltage may bring into breakdown of the isolation barrier or shock hazard problem to users. However, the operating frequency in power conversion circuit is not usually designed beyond 1 MHz because of cost limitation in gate drivers and power switches. Thirdly, if the effective link capacitance is as small as the main switch output capacitance, the soft switching region shrinks and the zero voltage switching (ZVS) feature of the resonant operation may be lost [3].

With regard to these problems, trade-off studies between available coupling capacitance and maximum obtainable efficiency for a desired power was performed especially in a few MHz operating frequency where loss of the resonant inductor dominates [2]. They also suggested a primary automatic frequency tuning to regulate the output voltage and track the ZVS range. However, the resulting operating frequency increases relatively too high.

Other researchers introduced two L-type matching filters placed in the front-end and back-end of the link capacitors providing an increased power factor and a load current multiplication in order to handle more output power without increasing operating frequency too much [4]. Despite of its

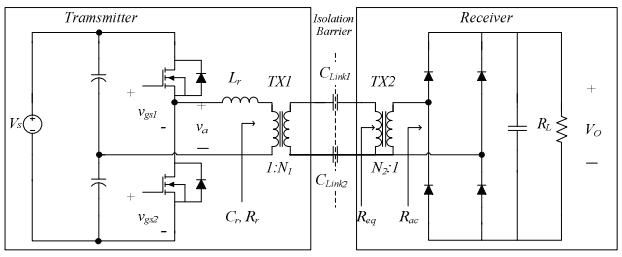


Fig. 1. Half-bridge resonant converter with double matching transformers

merits, additional five resonant components – three inductors and two capacitors should be designed and the design procedure based on iterative process become complex.

In the meanwhile, matching transformer scheme was introduced and its feasibility was partially verified and tested in [5] and [6], but there was no consideration on the voltage stress, operating frequency, and ZVS condition.

In this paper, as an effective driving method for CPT system with small link capacitance, half-bridge structure with double matching transformers is studied and the design guideline is investigated thoroughly.

II. Design Equations

A. Topology overview

Figure 1 shows a half-bridge converter with two matching transformers. While basic operation is similar to the conventional series resonant converter, the transformers inserted into the front and the rear side of the link capacitors, have dedicated functions. The input matching transformer, TX1, provides sufficient capacitance ratio to obtain ZVS operation and the output matching transformer, TX2, increases the effective load seen from the resonant tank in order to obtain high power factor in the transmitting circuit and to reduce the voltage stress in the link capacitances. Hence the determination of the circuit parameter is critical in the performance of the CPT system. The key design equations will be derived herein.

B. Output characteristics

For the analysis of operation, the normalized dc voltage gain is defined as

$$M = \frac{N_2 V_o}{N_1 V_g}(1+\gamma) \tag{1}$$

where Vo is the dc output voltage, Vg (=V_S/m) is the input voltage (m=2 for half-bridge), and N_1, N_2 are individual turn ratio of the primary and the secondary matching transformer, respectively. γ (=nV_F/Vo) is the rectifier voltage drop factor (n=2 for full-wave). The normalized operating frequency and resonant angular frequency are also defined by

$$F = \frac{\omega}{\omega_O} = \frac{f}{f_O} \tag{2}$$

and

$$\omega_O = \frac{1}{\sqrt{N_1^2 L_r C_e}}. \tag{3}$$

If every parameter is reflected into the switch side, The driving voltage source, V_a, is a square pulse with the peak to peak value of V_S (=2V_g) with the operating frequency of ω (=$2\pi f$). If the output filter capacitance, C_o, is very large, the output voltage can considered as a stiff voltage source and the load-side voltage reflected into the inverter-side, V_b, is in phase with the sinusoidal inductor current. Owing to the diode action of the rectifier stage and is in square waveforms with the amplitude of the output voltage amplified by the transformers' turn ratio. Assuming that the effective quality factor is sufficiently high and the operating frequency is always higher than the resonant frequency, the current through the resonant inductor can be regarded by a sinusoidal waveform and fundamental harmonic approximation(FHA) is possible [10][11]. In this case, the quality factor and the characteristic impedance of the resonant network are defined by

$$Q_e = \frac{Z_o}{R_{eq}}, Z_o = \sqrt{\frac{L_r}{N_1^2 C_e}}. \tag{4}$$

and the ac equivalent load including the full-wave rectifier reflected into the resonant tank is calculated as

$$R_{eq} = \left(\frac{N_2}{N_1}\right)^2 \frac{8}{\pi^2}\frac{V_o}{I_o}(1+\gamma) \tag{5}$$

where I_o are the dc output current.

The normalized dc voltage gain relation results in

$$M = \frac{1}{\sqrt{1+Q_e^2\left(F-\frac{1}{F}\right)^2}}. \tag{6}$$

With valid range of F≥1(above resonance operation) and 0<M≤1, F can be rearranged as follows.

$$F = \frac{1}{2Q_e}\sqrt{\frac{1}{M^2}-1}+\frac{1}{2}\sqrt{\frac{1}{Q_e^2}\left(\frac{1}{M^2}-1\right)+4} \tag{7}$$

Equation (7) says that, in order to regulate the constant output voltage, the normalized operating frequency should be controlled to make the dc voltage gain constant when the load changes.

C. Zero voltage switching condition

The series resonant LC tank can provide ZVS feature to the main MOSFET switches when is driven in the above resonance region. However the ZVS region is heavily dependent on the load condition and thus necessary condition for ZVS should be considered here. To achieve the zero voltage turn-on of the main MOSFET switch, the charge circulated during the commutation should be large enough to clear off the charge stored in the drain-source of switching MOSFETS. In other words, the ZVS condition is

$$q_{TANK} \geq q_{SW} \tag{8}$$

where q_{TANK} denotes the circulating charge in the resonant tank and q_{SW} is the stored charge at the instant of turn-on of the switch.

The main switch output capacitance, C_{oss} is mainly a pn-junction depletion capacitance which has a non-linear voltage dependency, and thus the equivalent linear capacitance in the full excursion of drain to source voltage can be obtained as

$$C_{sw} = \frac{1}{V_S}\int_0^{V_S} C_{oss}(v_{DS})dv_{DS} = 2C_{oss}\Big|_{v_{DS}=V_S} \tag{9}$$

Because, in half-bridge topology, both of the switch output capacitance are involved at the same time, total charge is calculated by

$$q_{SW} = 2C_{sw}V_S = 4C_{sw}V_g \tag{10}$$

Besides, assuming the fundamental component of the driving voltage, Va, is given by

$$v_{a1}(t) = V_{am}\cos\omega t\,, \tag{11}$$

the current through the inductor can be regarded as

$$i_L(t) = I_{Lm}\cos(\omega t - \phi) \tag{12}$$

where □ is the phase angle. If we define the input impedance, Zi(ω), looking into the resonant tank from the half-bridge switch, the phase of the input impedance is obtained by

$$\tan\phi(\omega) = Q_e\left(F - \frac{1}{F}\right). \tag{13}$$

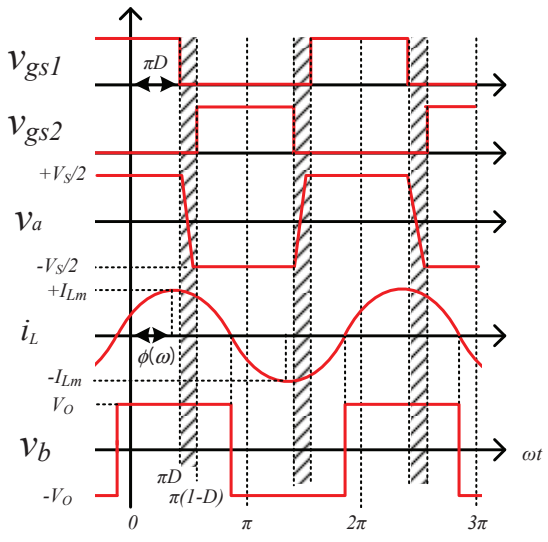


Fig. 2. Approximate waveforms for ZVS analysis

The circulating charge is calculated by the timing diagram in Fig. 2. Assume the duty cycle of the half-bridge converter as D, the integration of the inductor current in shaded dead-time duration is the charge displacement to provide soft-switching. By integrating the current from the turn-off instance of one switch to the turn-on instant of the other switch, q_{TANK} is obtained as

$$q_{TANK} = \frac{1}{\omega}\int_{\pi D}^{\pi(1-D)} i_L(\theta)d\theta = \frac{1}{\omega}2I_{Lm}\sin\phi(\omega)\cos\pi D\,. \tag{14}$$

Utilizing (13) and (14), the ZVS condition in (8) is then

$$N_1^2\kappa_{op} \geq \kappa \tag{15}$$

where κ is the capacitance ratio

$$\kappa \equiv \frac{C_{sw}}{C_e} \tag{16}$$

that is pre-determined by switch parasitic and mechanical energy link structure and κ_{op} is a function of operating point defined by

$$\kappa_{op} \equiv \frac{2}{\pi}\frac{(1-M^2)}{F^2}\cos\pi D\,. \tag{17}$$

Arranging (15), (16), and (17), the minimum turn-ratio, $N_{1,min}$, of the primary matching transformer can be obtained with respect to ZVS condition as follows.

$$N_{1,min} = \sqrt{\frac{\kappa}{\kappa_{op}}} \tag{18}$$

That is, ZVS is successfully achieved when N_1 is designed to be larger than $N_{1,min}$, or equivalently when N_2 is larger than $N_{2,min}$.

$$N_{2,min} = N_{1min}\frac{V_O M}{V_g(1+\gamma)} \tag{19}$$

In the design steps, if M is chosen to be near unity, very high value of turn ratio is required to achieve ZVS function. It should be also noted that the worst case ZVS condition occurs in the light load condition where F has its maximum value.

D. Voltage stress calculation in the link capacitors

In capacitive energy transfer system, it is very important to consider the withstanding voltage of the isolation barrier within the link capacitors. The voltage stress on the effective capacitance, V_{Cm}, can be obtained by the law of conservation of charge. Through the voltage swing from $-V_{Cm}$ to $+-V_{Cm}$, the total charge displaced by the resonant current is

$$q = C_e \cdot 2V_{Cm} \tag{20}$$

Besides, the output current is simply the rectified average value of the resonant current in the capacitor reflected into the load side. Therefore, the output current is

$$I_o = N_2 \frac{2}{T}\int_{half\ period} |\, i_{C_e}(t)\,|dt = N_2 \frac{2q}{T} \tag{21}$$

where T is the switching period. Equating (20) and (21) to eliminate q,

$$V_{Cm} = \frac{1}{4}\frac{I_O}{N_2}\frac{T}{C_e} \tag{22}$$

and eliminating the period which is dependent on the turn-ratio results in the following compact form.

$$V_{Cm} = \frac{4}{\pi}\frac{Q_e}{F} N_2 V_O \tag{23}$$

The voltage stress in the effective link capacitor is proportional to the turn-ratio, N_2, of the secondary matching transformer and mainly dependent on the quality factor, Qe, which is directly proportional to the load current. The worst case condition occurs in the heavy load which has the maximum Qe and the minimum F.

E. Switch stress calculation

Because the output current is simply the rectified average value of the resonant current in the inductor reflected into the load side, the following condition holds.

$$I_o = \frac{N_2}{N_1}\frac{2}{T}\int_{half\ period} |\, i_L(t)\,|dt \tag{24}$$

This equation states that the inductor current is directly proportional to the load current. Substituting (12) into (24), the maximum current stress in the inductor is obtained.

$$I_{Lm} = \frac{\pi}{2}\frac{(1+\gamma)}{M}\frac{V_O I_O}{V_g} \tag{25}$$

In order to minimize it, M should be minimized.

F. Operating frequency

To complete the design, we need another thing to consider. Practically, the maximum operating frequency is limited by gate driver and the minimum operating frequency is limited by the magnetic flux involved. Because the maximum and the minimum operating frequency occurred in the light and the heavy load condition respectively, combining (9), (10), (11), and (12), the resonant frequency is obtained by

$$f_O = \frac{\pi}{16}\frac{I_O}{V_O(1+\gamma)C_e Q_e}\cdot\frac{1}{N_2^2} \tag{26}$$

Therefore, the maximum and minimum operating frequency can be obtained.

III. DESIGN GUIDELINE

A. Design Procedure

The optimal design procedure is to find the component values, L_r, N_1, and N_2 which achieves the ZVS condition, minimizes the voltage stress in the isolation barriers, and minimizes the current stress for all operating load range. Using the normalized quantities, the design process is to properly select an operating point in the plane of N_2 vs. M curve – i.e. turn-ratio in the output matching transformer versus the normalized dc voltage gain. Because there are three unknown circuit parameters to be determined and only two design values are available, the third constraint may be helpful for design optimization. It is known that the resonant quality factor larger than unity guarantees the validity of FHA, the condition $Q_{e,min}$=1 will be adopted as the design constraint. With the valid load range, Q_{max} is directly calculated from the ratio of the minimum and the maximum load currents.

The design procedure starts from the capacitor voltage stress. Capacitor voltage stress is nearly proportional to N2. In view of the current stress, it is better to choose M as close to unity as possible because the current stress is inversely proportional to M. On the contrary, $N_{2,min}$ dramatically increases when M is approaching unity. Therefore, there is a design trade-offs among the current stress, the ZVS condition, and the capacitor voltage stress. The following summarizes the design steps.

- Step 1: Using (7) and (22), plot constant Vcm curves in N_2 vs M plane with heavy load assumption. From the maximum allowable voltage stress on the effective link capacitance, choose one trajectory of constant Vcm.
- Step 2: Plot the curve of $N_{2,min}$ in the same plane. Upper area of this boundary represents the ZVS region.
- Step 3: In order to achieve ZVS condition in the light and to minimize the current stress at the same time with a pre-determined voltage stress, choose the intersection point between the two curves drawn in Step 1 and 2 as the design point.
- Step 4: Calculate N_1 and L_r to complete the design.

B. Design Example

To verify the analysis and the design process, an energy link structure was constructed first by two pairs of plates having 10cm x 10cm in width and height, 0.2mm in gap filled with an insulation tape (ε_r = 3). The measured capacitance values of the link capacitors were 500pF and 526pF respectively, which altogether made the effective link capacitance 256pF.

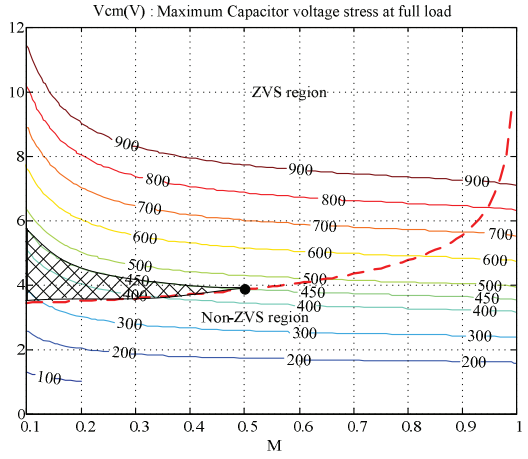


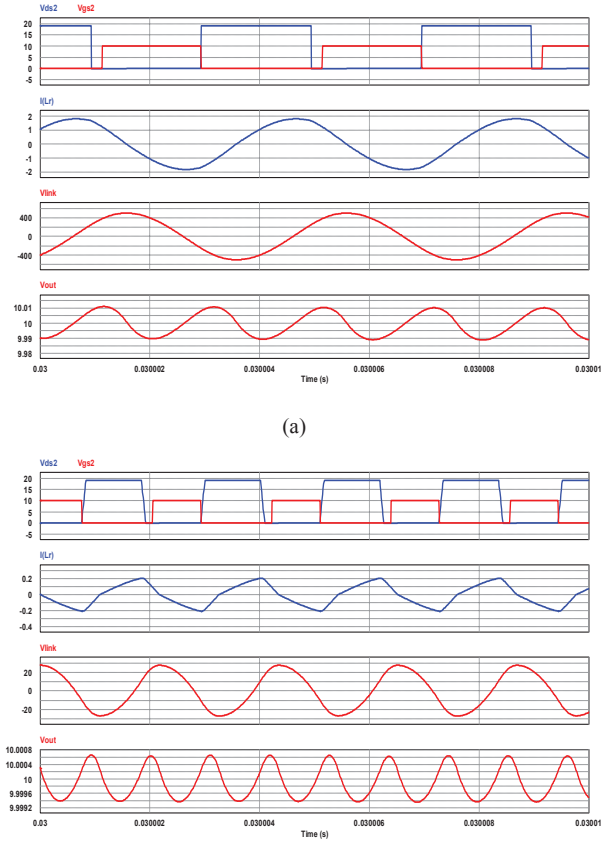
Fig. 3. Contour plot of V_{Cm} in N2-M plane (Vg=9.5, Vo=10,V_F=0.5 D=0.45)

Now, a 5W target wireless dc/dc conversion system from 19V input to 10V output, in which the minimum and the maximum load current were 50mA and 500mA, was considered. The equivalent linear capacitance of C_{sw}=400pF was calculated by (9) using datasheet value of the main MOSFET switch (FQPF20N60, 60V/15A).

Figure 3 shows the design curve of N_2 vs. M with various maximum capacitor voltage stress, V_{Cm} in case of heavy load which provides the worst condition for it. The red broken line indicates $N_{2,min}$ in the light load, which is boundary of ZVS operation. The V_{Cm} is linearly dependent on N2 and the slope changes from steep to gentle as M increases. The curve also shows that $N_{2,min}$ increases dramatically near unity M as mentioned before.

If we choose the maximum allowable voltage stress on the effective link capacitance is 450V. By design guideline, the design point (M,N2)=(0.5,3.9) is obtained. N_1=9.03 is obtained from (1) and (7) with the assumption of Qe,min=1. The resonant frequency is calculated by (26) as 229kHz and the resonant inductance is 23.1uH. The design equation predicts that the maximum voltage stress on the effective capacitor is 455V, the maximum inductor current stress is 1.82A, and the operating frequency is 249.7kHz in the full load condition. In the light load condition, the switching frequency will be increased to 501.5kHz.

To verify the performance, the designed circuit parameter values were implemented into PSIM circuit simulation software. The two power switches are modeled by an ideal MOSFET in parallel with an ideal diode and an linear equivalent switch capacitor of 400pF. Gate driver dead-time is set to 200nsec. Fig. 4(a) shows the simulation waveforms in the full load condition: The switching frequency is 249.3kHz and the estimated voltage stress in the effective link capacitor is 504V and maximum inductor current is 1.81A. The drain to source voltage of the low-side switch, Vds2 remains zero before the rising of gate signal, Vgs2, and thus zero voltage turn-on is successfully achieved in each switch. Fig. 4(b) shows the simulation waveforms in the light load condition.



(a)

(b)

Fig. 4. Simulation waveforms (a) full load (R_L=20Ω), (b) light load (R_L=200 Ω)

The switching frequency is 460.7kHz and the estimated voltage stress in the effective link capacitor is 50V and maximum inductor current is 0.205A.

In both cases, the output voltage is regulated to 10V. Furthermore, the drain to source voltage waveform of the low side MOSFET shows smooth transition during the dead time and thus verifies that ZVS operation at the instant of switch turn on is successfully achieved. The only discrepancy from the theoretical value is the 10% decrease in the maximum switching frequency in the light load condition. Fig. 4(b) shows the inductor current is slightly distorted in the light load, which causes a little error in FHA adopted in the theoretical analysis.

Figure 5 is the photograph of the hardware implementation of the CPT system. The primary plates of link capacitors were merged into the energizing table with a horizontal clearance of 4cm. The transmitter board contained an inverter and an input matching transformer. A receiving unit which had secondary plates of link capacitors, an output matching network, and a rectifier was mounted on the table with insulation paper of 0.2mm thickness.

In the inverter stage, the main switches were n-channel MOSFETs and the gate driver was IRS2186 with a dead time setting of 200nsec. In the rectifier stage, four Schottky diodes

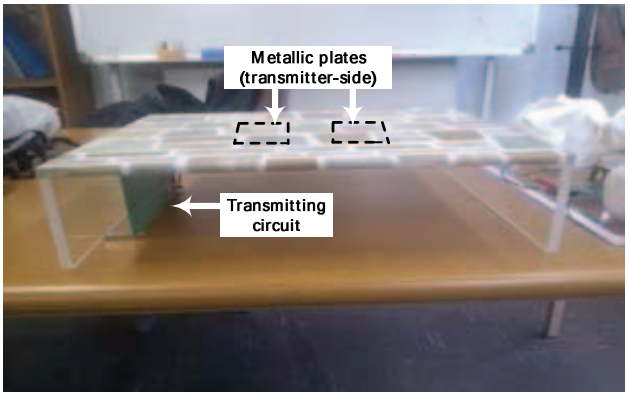
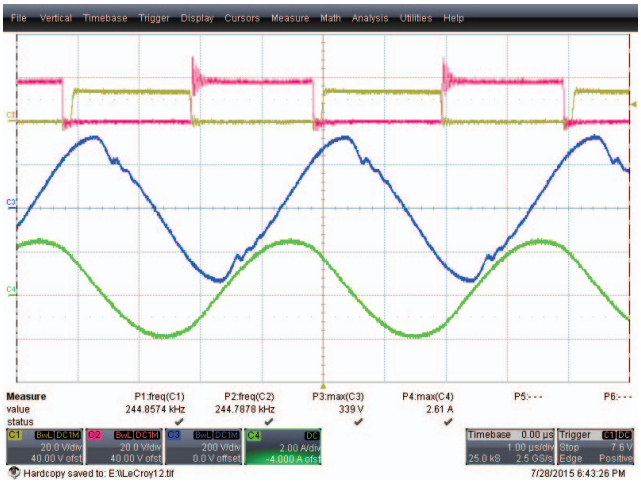
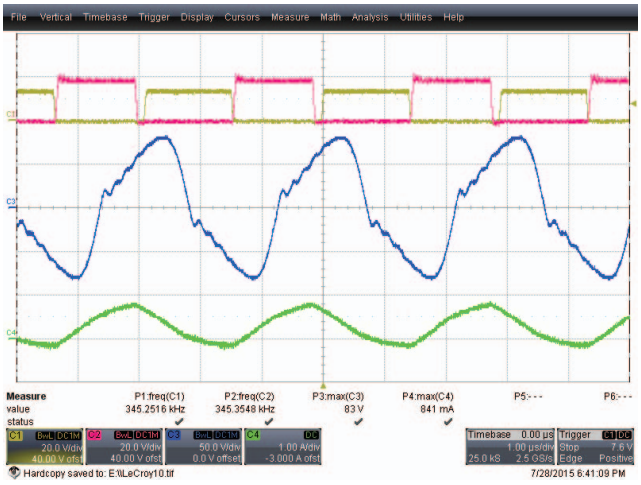


Fig. 5. Photograph of the energizing surface with link capacitors



(a)



(b)

Fig. 6. Hardware waveforms (a) full load (R_L=20Ω, Ch1: Vgs2@20V/div. Ch2:Vds2@20V/div. Ch3: Vclink@200V/div. Ch4: I_L@1A/div.) (b) light load (R_L=200Ω, Ch1: Vgs2@20V/div. Ch2: Vds2@20V/div. Ch3: Vclink@50V/div. Ch4: I_L@1A/div.)

(STPS5L40, 40V/5A) implemented a full-wave rectifier and the output capacitor was a 10uF electrolytic capacitor. For magnetic components, the resonant inductor was wound on EI3026 with 6 turns, TX1 on EI4035S with 14T:127T, TX2 on EE2519 with 33T:8.5T (Samwha, PL7 ferrite). The inductance value with the leakage inductance of 1.69uH constructs Lr as 21.6uH. The frequency control IC was NCP1395B and the transmitter side and the receiver side were isolated by the optical link to transmit error signal to implement frequency control.

Figure 6 shows the hardware test results in the heavy and light load condition. It presents the gate-to-source voltage of the high and the low side MOSFETs, the drain-to-source voltage of the low side switch, and the inductor current waveforms. The hardware waveforms show that ZVS condition has been achieved even in the light load which is the worst case condition for soft-switching in series resonant topologies. The overall efficiency of the CPT system is 55.4% at full load.

IV. Conclusion

In this paper, as a viable circuit topology for capacitive power transfer system with small link capacitance, a half-bridge inverter with double matching transformers has been investigated and implemented. With mathematical analysis, optimal design procedure has been proposed to achieve ZVS condition with reduced capacitor voltage. Simulation and hardware implementation have been performed to verify the analysis. Prototype 5W hardware equipped with an effective link capacitance of 256pF and switch output capacitance of 200pF operates successfully in ZVS condition up to 10% load with the switching frequency that ranges from 244.5kHz to 345.6kHz. The three magnetic components will be further simplified by merging the resonant inductor with TX1 in the subsequent study.

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